We Claim:

1. A memory circuit, comprising:

memory areas selected by a memory selection signal; and

a control circuit connected to and refreshing said memory areas in accordance with a refresh request signal, said control circuit:

in a first operating mode, carrying out the refreshing of one of said memory areas at a refresh address after receiving the refresh request signal and generating a refresh signal if an addressed memory area has been deselected or if, in an event of selection of said addressed memory area by the memory selection signal, access to said addressed memory area has ended before generation of a further refresh request signal;

in a second operating mode, interrupting the access to said addressed memory area for writing and reading-out of data and carrying out the refreshing of said address memory area by generating the refresh signal if said addressed memory area has been selected and the further refresh request signal has been received before an ending of the access to said addressed memory area after receiving the refresh request signal.

2. The memory circuit according to claim 1, wherein said control circuit contains a refresh circuit for refreshing said memory areas at predetermined refresh addresses depending on the refresh signal for retaining stored information.

3. The memory circuit according to claim 1, wherein said control circuit includes:

a refresh request counter being incremented by the refresh request signal; and

a refresh control circuit generating the refresh signal in dependence on a counter reading of said refresh request counter.

4. The memory circuit according to claim 3, wherein said control circuit has a refresh request circuit connected to said refresh request counter for generating the refresh request signal at predetermined times.

5. The memory circuit according to claim 3, wherein said refresh control circuit generates the refresh signal if the refresh request signal has been received and said address memory area is deselected or, in an event of selection of said addressed memory area by the memory selection signal, the

refreshing of said addressed memory area at the refresh address is possible during the access to said address memory area, or if said addressed memory area is selected and the further refresh request signal is received before an ending of the access to said addressed memory area.

6. The memory circuit according to claim 3, wherein said refresh request counter transmits a first refresh counter signal and a second refresh counter signal to said refresh control circuit.

7. The memory circuit according to claim 3, wherein said refresh control circuit is connected to said refresh request counter for decrementing said refresh request counter in an event of the generation of the refresh signal.

8. The memory circuit according to claim 1, wherein said memory areas have word lines.

9. The memory circuit according to claim 1, wherein the memory circuit is a psuedostatic memory circuit.

10. A method for operating a memory circuit, which comprises the steps of:

carrying out a refreshing process in a first operating mode for refreshing a memory area at a refresh address after receiving a refresh request signal if the memory area is deselected or if, in an event of a selection of said memory area, an access to the memory area is ended before a reception of a further refresh request signal; and

interrupting, in a second operating mode, the access to the memory area for writing and reading-out of data and performing the refreshing process of the memory area if the memory area is selected and the further refresh request signal is received before an ending of the access to the memory area.

11. The method for operating the memory circuit according to claim 10, which further comprises providing a pseudostatic memory circuit as the memory circuit.